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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,833	12/04/2001	Krishnaswamy Ramkumar	5298-06500	7743

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EXAMINER
DEO, DUY VU NGUYEN

ART UNIT	PAPER NUMBER
1765	3

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,833	RAMKUMAR ET AL.	
	Examiner	Art Unit	
	DuyVu n Deo	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *26-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *26-30* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-4, 6-15, 17-19, 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (US 6,410,403).

Wu describes a method for processing a shallow trench isolation comprising: polishing an upper layer of oxide layer 34A (claimed upper layer of the semiconductor topography) to expose silicon nitride layer 24A (claimed first underlying layer) (col. 3, line 49-53); etching

away remaining portion of the silicon nitride, this would expose the under sacrificial oxide layer 22 (claimed second underlying layer) (col. 3, line 55-60); polishing the oxide layer 34A (claimed planarizing the topography) (col. 3, line 61-62).

Referring to claim 10, the method further comprising: forming a trench extending through a stack, of intervening layers of different etching characteristics, including pad oxide, first nitride, sacrificial oxide, and second nitride layer (col. 3, line 19-35); blanket depositing oxide layer filling the trench and over the stack of layers (col. 3, line 40-44); planarizing the oxide layer such that the upper surface of the oxide layer, remaining within the trench, is coplanar with an upper surface of the adjacent layer of the stack, wherein the planarizing removes some of silicon nitride layer 24A of the stack (col. 3, line 49-53; figure 4).

Referring to claims 2 and 3, the polishing of the upper oxide layer removes the oxide layer arranged above the upper surface of the nitride layer 24A, which also polished (claimed first underlying layer) (figures 3, 4).

Referring to claim 4, since some of the nitride layer 24A is still on the substrate after the polishing (figure 4), this would show that the nitride layer's thickness is sufficient to prevent polishing through the nitride layer during the polishing of the upper layer.

Referring to claim 6, the oxide layer 34A (claimed upper layer) is deposited within the trench prior to the polishing (col. 3, line 40-51; figures 3, 4).

Referring to claim 7, since planarizing the oxide layer such that the upper surface of the oxide layer is remained within the trench and is coplanar with an upper surface of the adjacent layer of the stack (figure 4), this would read on claimed polishing the upper layer such that remaining portions of the upper layer are laterally confined by sidewalls of the trench.

Referring to claims 8 and 9, the method further comprises etching the planarized substrate such that the oxide layer 22, (claimed second underlying layer) and first nitride layer 18 (claimed third underlying layer), underneath the oxide layer 22, is removed (col. 3, line 59, 60; col. 4, line 5).

Referring to claims 11 and 19, the method comprises: polishing the oxide layer 34 (figure 3) to expose an upper nitride layer 24A (figure 4) of the stack; etching away remaining portion of the nitride layer, this would expose the under sacrificial oxide layer 22 and the nitride layer 18 (any of these layer would read on claimed intermediate layer) (col. 3, line 55-60); subsequently polishing the oxide layer and the nitride layer 18, this would certainly expose the upper surface of the nitride layer 18 (upper surface of the adjacent layer of the stack) and read on claimed polishing the topography to expose upper surface of the adjacent layer of the stack (col. 3, line 60-65). The nitride 18 is a lower layer of the stack.

Referring to claim 12, figure 6 shows that there is no dishing of the adjacent layer of the stack during the subsequently polishing step.

Referring to claims 13 and 14, the upper silicon nitride layer thickness is about 200-1500 angstrom prior to the planarizing step, this includes claimed 500-1000 angstrom (col. 3, line 28-30).

Referring to claim 15, the nitride layer 18 (intermediate layer) has a thickness of 600-1000 angstroms prior to the planarizing step (col. 3, line 22-23). This includes claimed approximately 300-700 angstroms.

Referring to claim 17, sacrificial oxide layer 22 (intermediate layer) and the oxide layer 34 would have similar etch characteristics since they are both oxide.

Referring to claims 18, 19, and 21, the adjacent layer is silicon nitride 18 (lower layer or intermediate layer).

Referring to claim 22, the method further comprising etching the nitride layer 24A and sacrificial oxide layer 22 (col. 3, line 55-60), this would read on claimed etching the upper surface of the adjacent layer to expose the semiconductor substrate.

Referring to claims 23 and 24, since the total thickness of nitride layer 24A and oxide layer 22 that is removed is about 150-400 angstrom (col. 3, line 24, 25, 50-53) and the oxide layer is coplanar with the nitride layer 24A prior to the etching, the oxide layer that extends above the upper surface of the semiconductor substrate subsequent to the etching step would be from 150-400 angstrom, this would read on claimed less than 500 angstrom or between 300-500 angstrom.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu as applied to claim 1 above, and further in view of Yieh et al. (US 6,114,216) and Chou et al. (US 6,348,389).

Unlike claimed invention, Wu doesn't describe forming the oxide layer 34 (upper layer), nitride layer 24 (first underlying layer), and the oxide layer 22 in a single process chamber. Yieh suggests to perform multiple process steps in situ in a same chamber during the producing of shallow trench isolation (col. 7, line 23-25). Chou, on the other hand, shows that these oxide and

nitride layers can be formed in the same chamber (col. 4, line 22-25). It would have been obvious for one skill in the art at the time of the invention to modify Wu in light of Yieh and Chou to form these oxide, nitride layers in a same chamber because Yieh suggests that performing multiple process steps in the same chamber would reduce total processing time, ensure high quality processing, increases the control over process parameters, reduce moisture content in deposited film, and minimizes device damage due to metal or impurities contamination or process residue contamination (col. 7, line 22-33; col. 54, line 11-18).

5. Claims 20, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu.

Unlike claim 20, Wu doesn't describe the nitride layer 18 (lower layer) has a thickness of approximately 300-500 angstrom prior to planarizing. However, he describes that the specific details are set forth such as thicknesses in order to provide a more thorough understanding of the invention. It is obvious to one skill in the art that the invention may be practiced without these details (col. 4, line 44-54). Therefore, it would be obvious to one skill in the art that the thickness would have to be determined through routine experimentation in order to provide optimum nitride thickness to produce shallow trench isolation with a reasonable expectation of success.

Unlike claim 20, Wu doesn't describe the shallow trench isolation having trenches. However, it is well known to any skill in the art that a semiconductor device would have more than one trench and Wu further teaches that the singular forms "a", "an", and "the" includes plural referents (col. 4, line 36-4). Therefore, it would be obvious to one skill in the art to produce a plurality of trenches. Furthermore, since the method described by Wu includes the same steps as that of claimed invention as described above, his process would produce the

average thicknesses of upper portions of the oxide layer 34A (dielectric layer) extending above the semiconductor substrate and corresponding to each of the trenches differ by less than approximately 10%.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu as applied to claim 11 above, and further in view of Wolf et al. (Silicon Processing for the VLSI Era).

Unlike claimed invention, Wu doesn't describe the oxide 22 (intermediate layer) is silicon dioxide. However, he describes removing the oxide with dilute HF (col. 3, line 59-60). It is known to one skill in the art that silicon dioxide is removed by dilute HF as shown here by Wolf (pages 532-533). Therefore, it would have been obvious to one skill in the art that Wu refers the oxide 22 would be silicon dioxide because it is an oxide layer and removed by dilute HF. Using silicon dioxide would produce claimed invention with a reasonable expectation of success.

7. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-25, drawn to a method, classified in class 438, subclass 689.

II. Claims 26-30, drawn to a product, classified in class 257, subclass 499.

The inventions are distinct, each from the other because of the following reasons:

8. Inventions in group I and group II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process such as one that does not require the step of planarizing the topography.

9. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

10. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

11. During a telephone conversation with Kevin Duffer on 7/8/03 a provisional election was made with traverse to prosecute the invention of the method, claims 1-25. Affirmation of this election must be made by applicant in replying to this Office action. Claims 26-30 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

12. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 703-305-0515.

DVD